This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims

1. (Amended) A memory module, comprising:

a plurality of conductors, each of which have opposed first and second ends;

a stacked pair of integrated circuits coupled to the first end of each of the plurality of conductors; and

a molded resin encasing the stacked pair of integrated circuits and having an outer surface on which the second end of each of the plurality of conductors terminate in a ~~single~~ row near an edge of the memory module, and wherein the second end of each of the plurality of conductors is adapted for slideable engagement into a receptor.

2. (Original) The memory module as recited in claim 1, wherein the molded resin extends at least partially around the integrated circuit to form an entire outer dimension of the memory module.

3. (Original) The memory module as recited in claim 1, wherein the bonding pads of a first one of the stacked integrated circuits are coupled to the bonding pads of a second one of the stacked integrated circuits.

4. (Original) The memory module as recited in claim 1, wherein a lower surface of the first one of the stacked integrated circuits is bonded to an upper surface of a conductive plate, and wherein the opposite surface of the conductive plate extends flush with or beyond the outer dimension of the stacked pair of integrated circuits.

5. (Original) The memory module as recited in claim 1, further comprising a first set of wires extending between a plurality of bonding pads on one or both of the integrated circuits and the first end of a first set of the plurality of conductors.

6. (Original) The memory module as recited in claim 5, further comprising a second set of wires that transmit power and ground signals only extending between bonding pads of one or both of the integrated circuits and a first end of a second set of the plurality of conductors.

7. (Original) The memory module as recited in claim 1, wherein the plurality of conductors comprises flattened metal strips formed as part of a lead frame.

8. (Original) The memory module as recited in claim 1, wherein the first one of the pair of integrated circuits comprises storage elements and the second one of the pair of integrated circuits comprises a controller.

9. (Amended) A memory module, comprising:

a stacked pair of integrated circuits, wherein a first one of the pair of integrated circuits comprises storage elements and a second one of the pair of integrated circuits comprises a controller;

a lead frame comprising a first portion and a second portion, wherein the first portion is configured below the stacked pair of integrated circuits and the second portion comprises a plurality of conductors coplanar with and extending laterally outside of the first portion;

a first set of wires extending between the stacked integrated circuits and a first set of the plurality of conductors; ~~and~~

a second set of wires which transmit power and ground signals only extending between the stacked integrated circuits and the first portion; and

wherein the memory module is mechanically and electrically interchangeable with a memory card.

10. (Original) The memory module as recited in claim 9, wherein the first one of the pair of integrated circuits comprises a controller and the second one of the pair of integrated circuits comprises a three dimensional array of storage elements.

11. (Original) The memory module as recited in claim 9, wherein the plurality of conductors have opposed first and second ends.

12. (Withdrawn) The memory module as recited in claim 11, wherein an outer edge of the memory module is adapted for slideable engagement into a receptor that is electrically connected to an electronic system.

13. (Withdrawn) The memory module as recited in claim 12, wherein the first end of each of the plurality of conductors is adapted to couple with the stacked integrated circuits, and wherein the second end of each of the plurality of conductors is adapted for frictional engagement with, and electrical connection to, conductive elements arranged within the receptors, during times when the edge of the memory module is slid into the receptor.

14. (Original) The memory module as recited in claim 9, wherein the first set of conductors is spaced laterally from the first portion, and wherein a second set of conductors is laterally coupled to the first portion.

15. (Original) The memory module as recited in claim 14, wherein the first portion comprises power and ground planar elements, and wherein the second set of conductors extend from and couple with the power and ground elements.

16. (Original) The memory module as recited in claim 15, wherein the power element extends as a ring coplanar with and laterally spaced from the ground element, and wherein at least a first one of the second set of conductors is coupled between a power supply and the ring, and wherein at least a second one of the second set of conductors is coupled between a ground supply and the ground element.

17. (Original) The memory module as recited in claim 9, further comprising a molded resin extending completely around the integrated circuits to form an entire outer dimension of the memory module and whereby the entire outer dimension of the memory module is of equivalent size to a memory card.

18. (Amended) The memory module as recited in claim 9, wherein the ~~memory module is mechanically and electrically interchangeable with a memory card, and wherein the~~ entire outer dimension of the memory module except for the second end of the plurality of conductors is surrounded by a covering that employs a mechanical tab which, when actuated, prevents writing data to the integrated circuits.

19. (Original) The memory module as recited in claim 9, wherein a surface of the first one of the stacked integrated circuits is bonded to a surface of the first portion of the lead frame, wherein the first portion extends flush with or beyond the outer dimension of the integrated circuits.

20. (Original) The memory module as recited in claim 9, wherein a set of bonding pads of the first one of the stacked integrated circuits is coupled to a set of bonding pads of the second one of the stacked integrated circuits.

21. - 31. (Canceled)